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EXAMINER	
ARORA, AJAY	
ART UNIT	PAPER NUMBER
2892	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/802,566	LIN, MOU-SHIUNG	
	Examiner	Art Unit	
	AJAY K. ARORA	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/3/08*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,7,9-12,15,17-19,21,22,25,27,29,30,91,96-99 and 101-103* is/are pending in the application.

4a) Of the above claim(s) *4,29 and 30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1,7,9-12,15,17-19,21,22,25,27,91,96-99 and 101-103* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 7 and 91 are rejected under 35 U.S.C. 103(a) as being unpatentable over IDS reference Malladi (US 5,629,240), hereinafter Malladi, with Feustel (US 2002/0008967) provided as evidence per applicant's request of 07/03/2008

Regarding claim 1, Malladi (refer to Figures 2A and 2B) teaches a circuit chip with multiple wirebonds (42 and 44) comprising:

a semiconductor substrate (14);

a transistor (10) in and on said semiconductor substrate;

multiple metal (22, 24') and dielectric (28, 30) layers over said semiconductor substrate;

a first contact pad (72) over said semiconductor substrate;

a second contact pad (70) over said semiconductor substrate;

a passivation layer (32) over said multiple metal and dielectric layers, wherein a first opening in said passivation layer is over said first contact pad and exposes said

first contact pad, and wherein a second opening in said passivation layer is over said second contact pad and exposes said second contact pad;

a power metal structure (not shown but connected to 72, Col. 6, lines 1-3) over said passivation layer and on said first contact pad, wherein said power metal structure is connected to said first contact pad through said first opening, wherein said power metal structure comprises a metal layer, and wherein one of said multiple wirebonds is bonded on said power metal structure (see Col. 5, lines 63-67 and Col. 6, lines 1-3);

a ground metal structure (not shown but connected to 70, Col. 6, lines 1-3) over said passivation layer and on said second contact pad, wherein said ground metal structure is connected to said second contact pad through said second opening, wherein said ground metal structure comprises a metal layer, and wherein another one of said multiple wirebonds is bonded on said ground metal structure (see Col. 5, lines 63-67 and Col. 6, lines 1-3);

a capacitor (74) over said passivation layer and directly over said first contact pad exposed by said first opening (Col. 6, lines 4-5);

a first solder connection (Col. 6, lines 6-8) connecting said capacitor to said power metal structure (connected to 72) ; and

a second solder connection (Col. 6, lines 6-8) connecting said capacitor to said ground metal structure (connected to 70).

Malladi does not teach that the said power metal structure and the said ground metal structure each comprise a “copper” layer. However, the use of copper for metallization, including power or ground metallization layer, is well known in the art. As

evidence, one may refer to Feustel (US 2002/0008967), page 1, paragraph 0012, which teaches a power metal structure including passive components soldered to metallization, wherein the metallization comprises copper. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Malladi so that the said power metal structure and the said ground metal structure each comprise a copper layer. The ordinary artisan would be motivated to modify Malladi at least for the purpose of using a high thermal and electrical conductivity metal for the power and ground metal structure for efficient power distribution with minimal losses.

Regarding claim 7, Malladi teaches substantially the claimed structure but does not teach that said ground metal structure further comprises “a gold layer" over said copper layer of said ground metal structure. However, the use of a gold layer, such as a gold plating, over a copper metallization layer is well known in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Malladi so that said ground metal structure further comprises a gold layer over said copper layer of said ground metal structure. The ordinary artisan would be motivated to modify Malladi at least for the purpose of providing a layer that has excellent resistance to corrosion.

Regarding claim 91, Malladi teaches that said passivation layer may comprise silicon nitride (Col. 1, lines 62-65).

3. Claims 15, 17-19, 21, 22, 25, 27, 97, 101, 102 and 103 are rejected under 35 U.S.C. 103(a) as being unpatentable over Malladi in view of Greer (US 6,451,681) of prior record, hereinafter Greer.

Regarding claim 15, Malladi (refer to Figures 2A and 2B) teaches an integrated circuit chip with a wirebonds (42 or 44), comprising:

a semiconductor substrate (14);

a transistor (10) in and on said semiconductor substrate;

multiple metal (22, 24') and dielectric (28, 30) layers over said semiconductor substrate;

a first contact pad (24') over said semiconductor substrate;

a passivation layer (32) over said multiple metal and dielectric layers, wherein a first opening (64, see Figure 2A) in said passivation layer is over said first contact pad and exposes said first contact pad;

a second contact pad (70) connected to said first contact pad through said first opening;

a third contact pad (not shown, but described as a peripheral pad in Col. 5, lines 57-63) connected to said first contact pad through said first opening and connected to said second contact pad, wherein the position of said third contact pad from a top perspective view is different from that of said first contact pad (because third contact pad is located at nearer to the periphery of the chip than the first contact pad, see Col.

5, lines 57-63), and wherein said wirebond (42) is bonded on said third contact pad (see Col. 5, lines 57-63);

a capacitor (74) over said passivation layer and over said second contact pad; and

a solder connection (Col. 6, lines 6-8) between said second contact pad and said capacitor, wherein said solder connection connects said capacitor to said second contact pad.

Malladi does not teach "a first polymer layer" over said passivation layer and hence does not teach "a second opening" in "said first polymer layer is over said second contact pad and exposes said second contact pad" or that the capacitor is "over said first polymer". Greer (refer to Figure 4) teaches a top level contact pad (312) in an electronic component with a first polymer layer (302) over a passivation layer (300) such that both the passivation layer and first polymer layer have an opening over the contact pad (312) and exposes the contact pad. If the first polymer layer (302) of Greer is incorporated into Malladi, the combination would now teach a first polymer layer over said passivation layer, wherein a second opening in said first polymer layer is over said second contact pad and exposes said second contact pad; and also the capacitor will be over said first polymer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Malladi in view of Greer as above. The ordinary artisan would be motivated to modify Malladi at least for the purpose of providing an additional protection layer over the metallization but providing openings in

the polymer layer (just like openings in passivation layer) as required to form interconnections.

Regarding claim 17, Malladi teaches substantially the claimed structure but does not teach that said second contact comprises a “gold” layer. However, the use of a gold layer, such as a gold plating, over a contact metallization layer is well known in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Malladi so that said second contact comprises a gold layer. The ordinary artisan would be motivated to modify Malladi at least for the purpose of providing a layer that has excellent resistance to corrosion.

Regarding claim 18, Malladi teaches substantially the claimed structure but does not teach that said second contact comprises a “copper” layer. However, the use of copper for contact metallization is well known in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Malladi so that said second contact comprises a copper layer. The ordinary artisan would be motivated to modify Malladi at least for the purpose of using a high thermal and electrical conductivity metal for the second contact to minimize electrical losses and improved functionality.

Regarding claim 19, Malladi (refer to Figures 2A and 2B) teaches a ground metal structure (Col. 6, lines 1-3)) connected to said capacitor, to said wirebond (42) and to said first contact pad (24').

Regarding claim 21, Malladi (refer to Figures 2A and 2B) teaches a power metal structure (Col. 6, lines 1-3) connected to said capacitor, to said wirebond and to said first contact pad (24').

Regarding claim 22, Malladi (refer to Figures 2A and 2B) teaches that said second contact pad (70) is over said passivation layer (32).

Regarding claim 25, Malladi teaches that said passivation layer may comprise silicon nitride (Col. 1, lines 62-65).

Regarding claim 27, Malladi teaches substantially the claimed structure but does not teach that said third contact comprises "gold". However, the use of a gold, for example gold plating, over a contact metallization is well known in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Malladi so that said third contact comprises gold. The ordinary artisan would be motivated to modify Malladi at least for the purpose of providing a layer of a material like gold that has excellent resistance to corrosion.

Regarding claim 97, Malladi does not teach a polymer layer over the passivation layer and hence does not teach the third and fourth openings in the polymer layer. Greer (refer to Figure 4) teaches a top level contact pad (312) in an electronic component with a polymer layer (302) over a passivation layer (300) such that, an opening in said polymer layer is directly over an opening in the passivation layer, such that the above two openings together expose the underlying contact pad. If the polymer layer of Greer is incorporated into Malladi, the combination would now teach a polymer layer over said power and ground metal structures, wherein a third opening in said polymer layer is over said power metal structure (i.e. third opening in said polymer layer is directly above opening in passivation above power metal structure) and exposes said power metal structure, and a fourth opening in said polymer layer is over said ground metal structure and exposes said ground metal structure, and wherein said first solder connection connects said capacitor to said power metal structure through said third opening, and said second solder connection connects said capacitor to said ground metal structure through said fourth opening. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Malladi in view of Greer as above. The ordinary artisan would be motivated to modify Malladi at least for the purpose of providing an additional protection layer over the metallization but providing openings in the polymer layer (just like openings in passivation layer) as required to form interconnections.

Regarding claim 101, Malladi (refer to Figures 2A and 2B) teaches that said capacitor comprises a capacitor that is capable of functioning as a decoupling capacitor (Col. 5, lines 57-60).

Regarding claim 102, Malladi as modified above in view of Greer for claim 15, teaches substantially the claimed structure but does not teach "a third opening" in "said first polymer layer is over said third contact pad and exposes said third contact pad". Greer (refer to Figure 4) teaches a top level contact pad (312) in an electronic component with a first polymer layer (302) over a passivation layer (300) such that both the passivation layer and first polymer layer have an opening over the contact pad (312) and exposes the contact pad. If the first polymer layer (302) of Greer is incorporated into Malladi, the combination would now teach an opening in said first polymer layer over all pads to which interconnections have to be made; i.e. it would teach a third opening in said first polymer layer that is over said third contact pad and exposes said third contact pad It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Malladi in view of Greer as above. The ordinary artisan would be motivated to modify Malladi at least for the purpose of providing an opening in the first polymer layer that enables bonding of interconnects to the said third contact pad, thus providing electrical connectivity.

Regarding claim 103, Malladi as modified above in view of Greer teaches that the said first polymer layer (302 of Figure 4 of Greer) may comprise polyimide (Col. 5, lines 54-

59). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Malladi such that said first polymer layer comprises polyimide. The ordinary artisan would be motivated to modify Malladi at least for the purpose of providing a material that provides excellent resistance to corrosion and for which process controls for depositing thin layers are well established.

4. Claims 9-12, 98 and 99 are rejected under 35 U.S.C. 103(a) as being unpatentable over Malladi in view of Master (US 2003/0037959) of prior record, hereinafter Master.

Regarding claim 9, Malladi (refer to Figures 2A and 2B) teaches an integrated circuit chip comprising:

a semiconductor substrate (14);

a transistor (10) in and on said semiconductor substrate;

multiple metal (22, 24') and dielectric (28, 30) layers over said semiconductor substrate;

a first contact pad (20') over said semiconductor substrate;

a passivation layer (32) over said multiple metal and dielectric layers, wherein a first opening (64, see Figure 2A) in said passivation layer is over said first contact pad and exposes said first contact pad, and wherein said passivation layer comprises a nitride (Col. 1, lines 62-65);

a second contact pad (72) connected to said first contact pad through said first opening, wherein the position of said second contact pad from a top perspective view is different from that of said first contact pad (because contact pads 20' and 72 are of different size),

a capacitor (74) over said passivation layer and over said second contact pad (Col. 6, lines 4-5);

a solder connection (Col. 6, lines 6-8) between said capacitor and said second contact pad, wherein said solder connection connects said capacitor to second contact pad.

Malladi does not teach that said second contact pad comprises "a gold layer with a thickness greater than 1 micrometer" or "an additional metal layer" between said solder connection and said second contact pad. Master teaches a chip with contact pads to which components may be attached by solder connection, wherein there is an additional metal layer between said solder connection and said second contact pad (page 2, paragraph 0027). Further, Master also teaches that a contact pad may comprise a gold layer (page 2, para 0027), but does not specify that the gold layer may have a thickness "greater than 1 micrometer". However, the thickness of the gold layer is considered to involve routine optimization, which has been held to be within the level of ordinary skill in the art. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Malladi such that said second contact pad comprises a gold layer with a thickness greater than 1 micrometer and there is an

additional metal layer between said solder connection and said second contact pad. The ordinary artisan would be motivated to modify Malladi at least for the purpose of providing a gold layer that has optimal thickness for its intended purpose (such as providing resistance against corrosion, increasing wettability, etc.) for the given design and providing the additional metal layer to provide a barrier layer between the solder and the underlying device (page 2, para 0027).

Regarding claim 10, Malladi (refer to Figures 2A and 2B) teaches a third contact pad (not shown, but described as a peripheral pad in Col. 5, lines 57-63) exposed by a second opening in said passivation layer (pad has to be exposed by an opening in said passivation to wirebond to it), and a wirebond (44) on said third contact pad.

Regarding claim 11, Malladi (refer to Figures 2A and 2B) teaches a third contact pad (not shown, but described as a peripheral pad in Col. 5, lines 57-63) over said passivation layer, and a wirebond (44) on said third contact pad.

Regarding claim 12, Malladi (refer to Figures 2A and 2B) teaches a third contact pad (24') exposed by a second opening in said passivation layer, a fourth contact pad on said third contact pad (not shown, but described as a peripheral pad in Col. 5, lines 57-63), and a wirebond (42) on said fourth contact pad.

Regarding claim 98, Malladi (refer to Figures 2A and 2B) teaches that said capacitor comprises a capacitor that is capable of functioning as a decoupling capacitor (Col. 5, lines 57-60).

Regarding claim 99, Malladi (refer to Figures 2A and 2B) teaches that said nitride comprises silicon nitride (Col. 1, lines 62-65).

5. Claim 96 is rejected under 35 U.S.C. 103(a) as being unpatentable over Malladi in view of Efland (US 6020640), hereinafter Efland.

Regarding claim 96, Malladi teaches substantially the claimed structure but does not teach that said ground metal structure further comprises a "nickel layer" over said copper layer of said ground metal structure. Efland teaches that it is known in prior art that a nickel layer may be used over a copper layer (Col. 1, lines 29-39). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Malladi such that said ground metal structure further comprises a nickel layer over said copper layer of said ground metal structure. The ordinary artisan would be motivated to modify Malladi at least for the purpose of improving reliability of interconnecting to copper (Col. 1, lines 29-39).

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Response to Arguments

6. Applicant's arguments, see page 19, 1st and 2nd paragraph of applicant's response, filed 07/17/2007, with respect to 35 U.S.C 112 rejection of claims 1, 9 and 15 have been fully considered and are persuasive. It is noted that based on the applicant's argument, all typical transistors formed on a semiconductor substrate may be considered to be "in and over a semiconductor substrate", or (as recited in amended claims of 12/7/2007) "in and on a semiconductor substrate".

On pages 11-14 of applicant's response, applicant argues about the rejection of claims 1, 4, 7, 91, 96 and 97. On page 14, 1st paragraph, applicant refers to the rejection of claim 1 and requests evidence to show that a power or ground metal structure that comprises a copper layer and utilizes a solder for attachment of the recited component, was known in the art at the time of the claimed invention. In response, the rejection of claim 1 provides Feustel reference which is cited as the above requested proof (refer to rejection of claim 1 for details).

7. On pages 14-17, applicant presents arguments related to claims 9-12, 98 and 99. On page 16, last paragraph, applicant argues that "Malladi et al.'s forming a capacitor over a chip is believed to be not within the scope of the flip-chip process, as above recited by Master" and concludes that Master is "non-analogous to Malladi". In response to applicant's above argument that Master is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was

concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Master teaches a chip with contact pads to which components may be attached by solder connection, wherein there is an additional metal layer between said solder connection and said second contact pad (page 2, paragraph 0027), which is similar to the teachings of connecting a capacitor to a chip of Malladi.

8. On pages 17-20, applicant presents arguments related to claims 15, 17-19, 21, 22, 25, 27, 29, 30 and 101-103. On page 19, last paragraph, applicant argues that Greer reference does not teach the limitations of claim 15 because "Greer fails to teach, hint or suggest that the opening in the passivation layer 300, 500 or 704 and opening in the polymer layer 302, 502, or 706 may expose different contact pads. as currently claimed in Claim 15". This argument is not persuasive. Whereas Figure 4 of Greer illustrates one exposed contact pad (312), Greer is teaching that contact pads that have to be connected to an interconnect (400/402 of Figure 4 of Greer) have to be exposed by openings in the passivation layer (300) and first polymer layer (302). Given that integrated circuits have multiple contact pads (312); such as a second contact pad or third contact pad etc., that have to be connected to interconnects (like wirebonds comprising 402), Greer does teach the limitation "a second opening in said first polymer layer is over said second contact pad and exposes said second contact pad", as recited in claim 15.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AJAY K. ARORA whose telephone number is (571)272-8347. The examiner can normally be reached on Mon through Fri, 8am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. K. A./
Examiner, Art Unit 2892

/Thao X Le/
Supervisory Patent Examiner, Art Unit 2892